THAT WHICH IS CLAIMED IS:

1. A vertical MOSFET, comprising:

a semiconductor substrate having a plurality of semiconductor mesas therein that are separated by a plurality of deep stripe-shaped trenches that extend in parallel and lengthwise across said substrate in a first direction;

a plurality of buried insulated source electrodes in the plurality of stripe-shaped trenches; and

a plurality of insulated gate electrodes that extend in parallel across the plurality of semiconductor mesas and into shallow trenches defined in said plurality of buried insulated source electrodes.

2. The vertical MOSFET of Claim 1, wherein each of the plurality of semiconductor mesas comprises at least one base region that supports vertical inversion-layer channels along opposing sidewalls of a respective pair of deep stripe-shaped trenches.

3. The vertical MOSFET of Claim 2, further comprising a surface source electrode that extends on said semiconductor substrate, is electrically connected to said plurality of buried insulated source electrodes and ohmically contacts the at least one base region in each of the plurality of semiconductor mesas.

4. The vertical MOSFET of Claim 3, wherein the ohmic contacts between said surface source electrode and the base regions are made at upper surfaces of the plurality of semiconductor mesas.

5. The vertical MOSFET of Claim 1, wherein said plurality of insulated gate electrodes are stripe-shaped electrodes that extend lengthwise across said semiconductor substrate in a second direction orthogonal to the first direction.

6. A vertical MOSFET, comprising:

a semiconductor substrate having a drift region of first conductivity type therein;

first and second trenches that extend lengthwise in a first direction in said substrate and define a semiconductor mesa therebetween into which the drift region extends;

first and second buried insulated source electrodes that extend lengthwise in the first direction adjacent bottoms of said first and second trenches, respectively; and

first and second spaced-apart gate electrodes that each extend lengthwise in a second direction across the mesa and into upper portions of the first and second trenches.

7. The vertical MOSFET of Claim 6, wherein said first and second gate electrodes are spaced side-by-side relative to each other in the upper portion of the first trench; and wherein said first buried insulated source electrode extends upward from adjacent the bottom of said first trench into a space between said first and second gate electrodes.

8. The vertical MOSFET of Claim 7, wherein a first source region of first conductivity type and a first base region of second conductivity type extend laterally across a width of the mesa from a sidewall of the first trench to an opposing sidewall of the second trench.

9. The vertical MOSFET of Claim 8, further comprising a surface source electrode that ohmically contacts the first and second buried insulated source electrodes in the space between said first and second gate electrodes.

10. The vertical MOSFET of Claim 9, wherein the first source region and the first base region extend to a surface of the mesa located in the space between said first and second gate electrodes; and wherein the surface source electrode ohmically contacts the first source region and the first base region at the surface of the mesa.

11. The vertical MOSFET of Claim 6, wherein the first and second directions are orthogonal relative to each other.

12. A vertical MOSFET, comprising:

a semiconductor substrate having a drift region of first conductivity type therein;

first and second trenches that extend lengthwise in a first direction in said substrate and define a first semiconductor mesa therebetween into which the drift region extends;

a third trench that extends lengthwise in the first direction in said substrate and defines a second semiconductor mesa extending between said second and third trenches;

first, second and third insulating regions that line bottoms and sidewalls of said first, second and third trenches, respectively;

first, second and third buried source electrodes that extend lengthwise in said first, second and third trenches, respectively; and

a first insulated gate electrode that extends lengthwise in a second direction orthogonal to the first direction across the first and second mesas and into said second trench.

13. The vertical MOSFET of Claim 12, further comprising a second insulated gate electrode that is spaced from said first insulated gate electrode and extends lengthwise in the second direction across the first and second mesas and into said second trench.

14. The vertical MOSFET of Claim 13, further comprising first and second spaced-apart source regions of first conductivity type that extend in the second mesa and opposite said first and second insulated gate electrodes, respectively.

15. The vertical MOSFET of Claim 14, further comprising a surface source electrode that ohmically contacts said first and second source regions in a space between said first and second insulated gate electrodes.

16. The vertical MOSFET of Claim 15, further comprising a base region of second conductivity type that extends lengthwise in the first direction in the second mesa and ohmically contacts said surface source electrode in the space between said first and second insulated gate electrodes.

17. The vertical MOSFET of Claim 16, wherein said first and second source regions extend in and form respective P-N junctions with said base region and have lengths that are less than 10 microns.

18. The vertical MOSFET of Claim 17, wherein opposing ends of said first and second source region are spaced from each other by less than about 2 microns.

19. A vertical MOSFET, comprising:

a semiconductor substrate having a plurality of semiconductor mesas therein that are separated by a plurality of deep stripe-shaped trenches that extend in parallel and lengthwise across said semiconductor substrate in a first direction, with each of the plurality of semiconductor mesas having at least one base region and at least one source region therein;

a plurality of buried insulated source electrodes that extend in the plurality of deep stripe-shaped trenches, with a first of said plurality of buried insulated source electrodes having a plurality of shallow trenches therein arranged at spaced locations along the length of a first of the plurality of deep stripe-shaped trenches; and

a plurality of insulated gate electrodes that extend in parallel across the plurality of semiconductor mesas in a second direction that extends at a non-zero angle relative to the first direction, with each of said plurality of insulated gate electrodes extending sufficiently deep into a respective shallow trench within the first of said plurality of buried insulated source electrodes that at least one respective vertical inversion layer channel is established in a respective base region within a first of the plurality of semiconductor mesas extending adjacent the first of the plurality of deep stripe-shaped trenches when the vertical MOSFET is biased in a forward on-state mode of operation.

20. The vertical MOSFET of Claim 19, wherein said plurality of insulated gate electrodes are zigzag shaped.

21. The vertical MOSFET of Claim 19, wherein the non-zero angle is about 90 degrees.

22. The vertical MOSFET of Claim 19, further comprising a surface source electrode that is electrically connected to said plurality of buried insulated source electrodes and ohmically contacts the base region within the first of the plurality of semiconductor mesas.

23. A vertical MOSFET, comprising:

a semiconductor substrate having a plurality of semiconductor mesas therein that are separated by a plurality of deep stripe-shaped trenches that extend in parallel and lengthwise across said semiconductor substrate in a first direction, with each of the plurality of semiconductor mesas comprising a drift region, a transition region on the drift region, a base region on the transition region and a source region on the base region;

a plurality of buried insulated source electrodes that extend in the plurality of deep stripe-shaped trenches, with a first of said plurality of buried insulated source electrodes having a plurality of shallow trenches therein arranged at spaced locations along the length of a first of the plurality of deep stripe-shaped trenches; and

a plurality of insulated gate electrodes that extend in parallel across the plurality of semiconductor mesas in a second direction that extends at a non-zero angle relative to the first direction, with each of said plurality of insulated gate electrodes extending sufficiently deep into a respective shallow trench within the first of said plurality of buried insulated source electrodes that at least one respective vertical inversion layer channel is established in a respective base region within a first of the plurality of semiconductor mesas extending adjacent the first of the plurality of deep stripe-shaped trenches when the vertical MOSFET is biased in a forward on-state mode of operation.

24. A method of forming a vertical MOSFET, comprising the steps of:

forming a base region of second conductivity type in a semiconductor substrate having a drift region of first conductivity type therein that forms a P-N junction with the base region;

forming a source region of first conductivity type in the base region;

forming a deep trench having a first sidewall that extends adjacent the base region, in the semiconductor substrate;

lining the deep trench with a first electrically insulating layer;

refilling the lined deep trench with a trench-based source electrode;

selectively etching the trench-based source electrode to define a shallow trench therein and expose a first portion of the first electrically insulating layer that extends on the first sidewall of the deep trench;

selectively etching the first portion of the first electrically insulating layer to expose an upper portion of the first sidewall of the deep trench and reveal the base region;

lining the shallow trench with a gate insulating layer that extends on the exposed upper portion of the first sidewall of the deep trench and a bottom and sidewalls of the shallow trench;

forming a gate electrode that extends on a surface of the semiconductor substrate and extends into the lined shallow trench; and

forming a surface source electrode that electrically connects the trench-based source electrode, source region and base region together.

25. The method of claim 24, wherein said step of forming a surface source electrode is preceded by the steps of:

forming a blanket passivation layer on the semiconductor substrate; and

patterning the blanket passivation to define contact holes therein that expose the trench-based source electrode, source region and base region.

26. The method of claim 24, wherein the trench-based source electrode comprise polycrystalline silicon; and wherein said step of lining the shallow trench comprises thermally oxidizing the exposed upper portion of the first sidewall at a first rate and the bottom and sidewalls of the shallow trench at a second rate that is higher than the first rate.

27. The method of claim 26, wherein said thermally oxidizing step comprises thermally oxidizing an upper surface of the trench-based source electrode to define a surface oxide layer thereon; and wherein said step of forming a surface source electrode is preceded by the step of selectively etching a portion of surface oxide layer extending adjacent the gate electrode to expose a portion of the upper surface of the trench-based source electrode.

28. The method of claim 24, wherein said step of lining the shallow trench comprises thermally oxidizing the exposed upper portion of the first sidewall at a first rate and the bottom and sidewalls of the shallow trench at a second rate that is at least about equal to the first rate.

29. A method of forming a vertical MOSFET, comprising the steps of:

forming a semiconductor substrate having therein a drift region, a transition region on the drift region, a base region on the transition region and a source region on the base region;

forming a deep trench having a first sidewall that extends adjacent the base, transition and drift regions, in the semiconductor substrate;

forming a trench-based source electrode in the deep trench;

forming a shallow trench that exposes the base region and source region extending along the first sidewall, in the trench-based source electrode;

forming a gate oxide insulating layer on the exposed base region;

forming a gate electrode that extends on an upper surface of the semiconductor substrate and extends into the shallow trench; and

forming a surface source electrode that electrically connects the trench-based source electrode, source region and base region together.

30. The method of claim 28, wherein said step of forming a surface source electrode is preceded by the steps of:

forming a blanket passivation layer on the semiconductor substrate; and

patterning the blanket passivation to define contact holes therein that expose the trench-based source electrode, source region and base region.

31. The method of claim 29, wherein said step of forming a gate electrode comprises forming multiple stripe-shaped gate electrodes that extend across the trench-based source electrode in a direction orthogonal to a lengthwise direction of the deep trench; and wherein the surface source electrode electrically connects the trench-based source electrode, source region and base region at locations extending between the multiple stripe-shaped gate electrodes.

32. The method of claim 29, wherein the trench-based source electrode is separated from the first sidewall by a first electrically insulating layer; and wherein said step of forming a shallow trench comprises selectively etching a portion of the first electrically insulating layer exposed by the shallow trench using the trench-based source electrode as an etching mask.